WHAT IS CLAIMED IS:

1. A circuit board comprising:

a first conductive pad;

a second conductive pad;

a capacitive element connected between the first and the second conductive pads; and

a series-resonant impedance coupled to the first pad, the series-resonant impedance comprising a serpentine conductor and a tuning capacitance.

2. A circuit board as defined in Claim 1, wherein the serpentine conductor is formed from a conductor that is printed on the circuit board.

3. A circuit board as defined in Claim 2, wherein tuning capacitance is planar in form.

4. A circuit board as defined in Claim 3, wherein the tuning capacitance is printed on the circuit board.

5. A circuit board as defined in Claim 1, wherein the serpentine conductor comprises:

a plurality of substantially linear segments;

an originating segment coupling a first linear segment to the first pad;

a terminating segment coupling a second linear segment to the capacitance; and

a turn coupling two adjacent linear segments.

6. A circuit board as defined in Claim 1, wherein serpentine conductor comprises:

at least one intermediate linear segment;

a first turn coupling the originating segment to the first linear segment;

a second turn coupling the first linear segment to an intermediate linear segment; and

a second turn coupling an intermediate linear segment to the second linear segment.

7. A circuit board as defined in Claim 6, wherein the serpentine conductor has a length (L) and a width (W) and wherein the respective lengths of the turns establishes a space (S) between adjacent linear segment and wherein the number of turns is equal to N, and wherein S, L, W and N are chosen so that the serpentine conductor is at least approximately series resonant with the tuning capacitance at a significant frequency F^o.

8. A circuit board as defined in Claim 7, wherein the tuning capacitance is substantially rectangular.

9. A circuit board as defined in Claim 8, wherein the linear segments are respectively mutually parallel.

10. A computer system comprising:

a printed circuit board;

at least one integrated circuit device mounted on the printed circuit board, the integrated circuit device having a significant frequency, F_o;

an active conductor coupled to the integrated circuit device;

a reference conductor coupled to the integrated circuit device;

a first pad coupled to the active conductor;

a second pad coupled to the reference conductor;

a capacitor coupled between the first pad and the second pad; and

means coupled to the capacitor for attenuating signals at F_o, the means comprising a serpentine conductor and a tuning capacitance.

11. A computer system as defined in Claim 10, wherein the reference conductor provides a ground potential to the integrated circuit device.

12. A computer system as defined in Claim 11, wherein the active conductor supplies an operating voltage to the integrated circuit device.

13. A computer system as defined in Claim 11, wherein the active conductor supplies an operating signal to the integrated circuit device.

14. A computer system as defined in Claim 10, wherein tuning capacitance is printed on the circuit board in the form of a substantially rectangular plane.

15. A computer system as defined in Claim 14, wherein the tuning capacitance is coupled to the reference conductor.

16. A computer system as defined in Claim 14, wherein the serpentine conductor is printed on the printed circuit board.

17. A circuit board as defined in Claim 14, wherein the serpentine conductor comprises:

a plurality of substantially linear segments;

an originating segment coupling a first linear segment to the first pad;

a terminating segment coupling a second linear segment to the capacitance; and

a turn coupling two adjacent linear segment.

18. A circuit board as defined in Claim 17, wherein serpentine conductor comprises:

at least one intermediate linear segment;

a first turn coupling the originating segment to the first linear segment;

a second turn coupling the first linear segment to an intermediate linear segment; and

a second turn coupling an intermediate linear segment to the second linear segment.

19. A circuit board as defined in Claim 18, wherein the serpentine conductor has a length (L) and a width (W) and the respective lengths of the turns establishes the space (S) between adjacent linear segments and wherein the number of turns is equal to N, and wherein S, L, W and N are chosen so that the serpentine conductor is at least approximately series resonant with the capacitance at a significant frequency F_o.

20. A circuit board as defined in Claim 19, wherein the tuning capacitance is substantially rectangular.

21. A circuit board as defined in Claim 20, wherein the linear segments are respectively mutually parallel.

22. A method of enabling the suppression of spurious signals in electronic equipment, the method comprising:

attaching a discrete capacitor to a printed circuit board (PCB) between a power pad and a reference pad;

depositing an inductance on the PCB so that the inductance is connected at a first end to the power pad;

forming a tuning capacitance on the PCB so that the tuning capacitance is connected to a second end of the inductance; and

causing the inductance and tuning capacitance to be dimensioned so that the inductance and tuning capacitance are substantially series resonant at a predetermined frequency, F_o.

23. A method as defined in Claim 22, wherein the inductance is deposited to form:

a plurality of substantially linear segments;

an originating segment coupling a first linear segment to the first pad;

a terminating segment coupling a second linear segment to the capacitance; and

a turn coupling two adjacent linear segments.

24. A method as defined in Claim 23, wherein the inductance is deposited to form:

at least one intermediate linear segment;

a first turn coupling the originating segment to the first linear segment;

a second turn coupling the first linear segment to an intermediate linear segment;

a second turn coupling an intermediate trace to the second trace; and

a third turn coupling an intermediate segment to the second trace.

25. A method as defined in Claim 24, wherein the inductance is deposited in a manner so that:

(i) the inductance has a length (L) and a width (W);

(ii) respective lengths of the turns establishes a space (S) between adjacent linear segments;

(iii) the number of turns is equal to (N); and

(iv) S, L, W, S and N establish a magnitude of the inductance such that the inductance is at least approximately series resonant with the tuning capacitance at F_o.

26. A method as defined in Claim 23, wherein the tuning capacitance is formed by depositing a planar conductor on a first surface of the PCB and positioning the planar conductor in proximity with a ground plane.

27. A method as defined in Claim 26, wherein the inductance is deposited to form:

at least one intermediate linear segment;

a first turn coupling the originating segment to the first linear segment;

a second turn coupling the first linear segment to an intermediate linear segment;

a second turn coupling an intermediate linear segment to the second linear segment; and

a third turn coupling an intermediate segment to the second linear segment.

28. A method as defined in Claim 25, wherein the inductance is deposited in a manner so that:

(i) the inductance has a length (L) and a width (W);

(ii) respective lengths of the turns establishes a space (S) between adjacent linear traces;

(iii) the number of turns is equal to (N); and

(iv) S, L, W, S and N establish a magnitude of the inductance such that the inductance is at least approximately series resonant with the tuning capacitance at F_o.

29. In an electronic equipment, a circuit for attenuating spurious signals at high frequencies, the circuit comprising:

a power pad;

a reference pad;

a discrete capacitor coupled between the power pad and the reference pad;

a ground plane; and

a printed circuit LC network connected to the power pad and coupled to the ground plane, and resonant at a predetermined frequency of a spurious signal, the LC network comprising:

a capacitive element;

a plurality of substantially linear segments;

an originating segment coupling a first linear segment to the power pad;

a terminating segment coupling a second linear segment to the capacitive element; and

a turn coupling two adjacent linear segments.

30. A circuit as defined in Claim 29, wherein the LC network further comprises:

at least one intermediate linear segment;

a first turn coupling the originating segment to the first linear segment;

a second turn coupling the first linear segment to an intermediate linear segment;

a second turn coupling an intermediate linear segment to the second linear segment; and

a third turn coupling an intermediate segment to the second linear segment.

31. A circuit as defined in Claim 29, wherein the capacitive element is formed by affixing a planar conductor on a first surface of a printed circuit board in proximity with the ground plane.

32. A circuit as defined in Claim 31, wherein the ground planes is affixed to a second surface of the printed circuit board.

33. A circuit as defined in Claim 31, wherein the LC network further comprises:

at least one intermediate linear segment;

a first turn coupling the originating segment to the first linear segment;

a second turn coupling the first linear segment to an intermediate linear segment;

a second turn coupling an intermediate linear segment to the second linear segment; and

a third turn coupling an intermediate segment to the second linear segment.

34. A circuit as defined in Claim 34, wherein the linear segments are mutually substantially parallel.

35. A circuit as defined in Claim 33, wherein the printed circuit LC network comprises a number, N, substantially linear segments, each having a width, W, and mutually-spaced from an adjacent linear segment by a distance, S, where N, W and S are chosen to form an inductance that in combination with the capacitive element and the discrete capacitor effects substantial attenuation at the predetermined frequency.

36. In an electronic equipment, a circuit module comprising:
a printed circuit board having a top surface and a bottom surface;
a first conductive pad;
a second conductive pad;
a ground plane;
a capacitor coupled between the first and the second conductive pads; and
means, including an inductance and a capacitance, coupled to the first pad for suppressing spurious signals at a predetermined frequency.

37. A circuit module as defined in claim 36, wherein the means consists essentially of a conductive trace disposed on the printed circuit board.

38. A circuit module as defined in Claim 1, wherein the means comprises:
a plurality of substantially linear segments;
an originating segment coupling a first linear segment to the first pad;
a terminating segment coupling a second linear segment to the capacitance; and
a turn coupling two adjacent linear segments.

39. A circuit module as defined in Claim 39, wherein the means comprises:
at least one intermediate linear segment;
a first turn coupling the originating segment to the first linear segment;
a second turn coupling the first linear segment to an intermediate linear segment; and
a third turn coupling an intermediate linear segment to the second linear segment.